REMARKS

Claims 25, 27-32, 34-37, 39-50, 52, and 53 are pending in this application, with all claims rejected. Previously, claims 1-24, 33 and 38 have been canceled and claims 26 and 51 have been withdrawn from consideration. By this Amendment, claims 29, 52, and 53 have been amended. In light of the amendments and remarks set forth below, Applicants respectfully submit that each of the pending claims is in immediate condition for allowance.

As an initial matter, claims 29, 52 and 53 stand rejected under 35 U.S.C. § 112, second paragraph. According to the rejection, use of the word "if" and the phrase "can no longer" in claims 29, 52, and 53 are not a positive recitation, and thus it cannot be determined if the condition will occur. To overcome these rejections, Applicants have amended these claims as shown above. These amendments were made for the sake of clarity and to place the application in a better condition for allowance. Therefore, withdrawal of these rejections is respectfully requested.

Applicants further note that the amendments to claims 29, 52, and 53 should overcome the rejection of claims 25, 27-32, 34-37, 39-50, 52, and 53 under 35 U.S.C. § 112, second paragraph, as being indefinite. Therefore, withdrawal of these rejections is respectfully requested as well.

The Office Action has also issued the following rejections, which Applicants respectfully traverse:

(1) Claims 25, 27-29, 34-37 and 45-50 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Inukai et al. ("Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration"; hereinafter "Inukai");

(2) Claims 30-32 and 52-53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Inukai in view of Matsuzaki et al. (U.S. Patent No. 6,500,715; hereinafter "Matsuzaki");

(3) Claims 39-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Inukai in view of Sani et al. (U.S. Patent No. 6,794,914; hereinafter "Sani");

(4) Claims 25, 27-32, 34-37 and 52-53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Oklobdzija et al. (U.S. Patent No. 6,232,810; hereinafter "Oklobdzija") in view of Matsuzaki; and

(5) Claims 39-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Oklobdzija in view of Matsuzaki and in further view of Sani.Claims 25, 27-29, 34-37, 45-50 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Inukai *et al.* (Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration; hereinafter "Inukai").

In particular, with regard to the rejection of claims 25, 27-29, 34-37, and 45-50 under 35 U.S.C. § 102(b), the Office Action relies on Fig. 9 of Inukai. Inukai, however, does not disclose (in Fig. 9 or anywhere else) at least two limitations recited in claim 29.

Specifically, claim 29 recites a plurality of switching transistors for coupling a flip-flop input signal into a storage flip-flop subcircuit. The Office Action takes the position that the "transistors within the set reset crossed coupled NAND gates" discloses this limitation. However, as shown in Fig. 9, the NAND gates form a flip-flop, and, therefore, cannot couple the flip-flop input signal, as claimed in the present application, into the characterized storage flip-flop subcircuit. The flip-flop input signal of claim 29 is generated "from an input signal and from a clock signal." In Fig. 9, the NAND gates receive a flip-flop input signal, but output Q and $\overline{Q}$, which are then stored on the characterized storage flip-flop subcircuit. Thus, the transistors within the set reset crossed coupled NAND gates provide a flip-flop output signal and do not disclose coupling a flip-flop input signal into a storage flip-flop subcircuit.

Applicants note that even if the set reset crossed coupled NAND gates coupled a flip-flop input signal into a storage flip-flop subcircuit, Inukai would still not disclose switching transistors as claimed in the present application. The terminals of the set reset crossed coupled NAND gates do not have a defined electrical potential in an operating state in which at least one supply voltage of the circuit arrangement is switched off as claim 29 requires. Instead, the set reset crossed coupled NAND gates go to an undefined "floating" electrical potential, which the circuit arrangement of the present application prevents. Such an arrangement enables a reliable retention of information stored in a storage flip-flops in a standby mode.

Claim 29 further recites an edge-triggered flip-flop comprising a storage flip-flop. The Office Action takes the position that the "six thick gate transistor on the right hand side" discloses a storage flip-flop. However, the six thick-gated transistors merely perform a storage function and do not disclose a storage flip-flop of an edge-triggered flip-flop. As explained above, the six thick-gated transistors receive a flip-flop output signal, that is, the logic functions are performed within the set reset crossed coupled NAND gates and not the six thick-gated transistors. The six thick-gated transistors merely store the output signal of the NAND gates. Further, since the six thick-gated transistors just store an output signal and are not part of the logic functionality of the circuit arrangement of Fig. 9, the information in the six thick-gated transistors has to be written back to the circuit's flip-flop (the set reset crossed coupled NAND gates) during the "wake-up process". (See Inukai, Fig. 9 & description.)

The circuit arrangement of the present application, however, does not require a wake-up process as both the logic and storage functions occur within the storage flip-flop of the edge-triggered flip-flop. As such, the six thick-gated transistors do not disclose a storage flip-flop of an edge-triggered flip-flop.

Accordingly, because Inukai fails to disclose all of the explicitly recited limitations recited in claim 29, Applicants respected submit that claim 29 is patentable over Inukai. Moreover,

since claims 27, 28, 34-37, and 45-50 ultimately depend on claim 29, the rejections of claims 27, 28, 34-37, and 45-50 should also be withdrawn.

Claims 52 and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Inukai in view of Matsuzaki. Although Applicants recognize that an obviousness inquiry is an expansive and flexible one, the Office Action must nevertheless demonstrate a prima facie case of obviousness to reject Applicants' claims for obviousness under 35 U.S.C. § 103(a). "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Manual of Patent Examining Procedure* § 706.02(j) (citing *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)).

Having argued that Inukai fails to disclose all of the limitations recited in claim 29, Applicants note that independent claims 52 and 53 include limitations similar in nature to that found in claim 29. In particular, claims 52 and 53 include the limitations of an an edge-triggered flip-flop comprising a storage flip-flop and a plurality of switching transistors for coupling a flip-flop input signal into a storage flip-flop subcircuit. Since, Inukai fails to disclose these limitations in claims 52 and 53 for at least the same reasons discussed above with respect to claim 29, and Matsuzaki does not cure this defect, the combination of Inukai and Matsuzaki does not disclose each and every element of claims 52 and 53. The proposed combination of Inukai and Matsuzaki therefore cannot establish a prima facie case of obviousness, and the rejections under 35 U.S.C. § 103(a) should be withdrawn.

Accordingly, for the foregoing reasons, Applicants respectfully request reconsideration and allowance of claims 52 and 53.

Claims 30-32 stand rejected for obviousness under 35 U.S.C. § 103(a) as being unpatentable over Inukai in view of Matsuzaki. Moreover, claims 39-44 also stand rejected for obviousness under 35 U.S.C. § 103(a) as being unpatentable over Inukai in view of Sani.

Claims 30-32 and 39-44 ultimately depend on claim 29. In rejecting these dependent claims, the Office Action relies on Inukai as disclosing all of the limitations recited in claim 29. As shown above, Inukai in fact does not disclose all of the limitations recited in claim 29. Because Inukai does not disclose all of the limitations recited in claim 29, and neither Matsuzaki nor Sani cure this defect, the combination of Inukai and Matsuzaki does not disclose each and every element of dependent claims 30-32. Accordingly, the rejections under 35 U.S.C. § 103(a) should be withdrawn.

In addition, claims 25, 27-29, and 34-37 stand rejected for obviousness under 35 U.S.C. § 103(a) as being unpatentable over Oklobdzija in view of Matsuzaki. In rejecting claim 29, the Office Action relies on FIG. 6A of Oklobdzija for disclosing all of the limitations of claim 29 except a first power switch transistor having a threshold voltage of a second value. Oklobdzija, however, does not disclose (in FIG. 6A or anywhere else) at least one other limitation recited in claim 29.

In particular, claims 29 recites a plurality of switching transistors for coupling a flip-flop input signal into a storage flip-flop subcircuit wherein each of the terminals of the switching transistors has a defined electrical potential in the operating state. The Office Action takes the position that the first logic block (34) and second logic block (36) of FIG. 6A discloses this limitation. However, the first logic block and second logic block form a flip-flop and do not couple a flip-flop input signal into the characterized storage flip-flop subcircuit. Instead, the first logic block and second logic block gates accept a flip-flop input signal ($\overline{S}$, $\overline{R}$, I_S, and/or I_R) and output two output signals (Q and $\overline{Q}$), which are then latched by the characterized storage flip-flop subcircuit. Thus, the transistors within the first logic block and second logic block provide an output signal and do not disclose or suggest coupling a flip-flop input signal into a storage flip-flop subcircuit.

Even if the first and second logic block coupled a flip-flop input signal into a storage flip-flop subcircuit, Oklobdzija would still not disclose or suggest switching transistors as claimed

in the present application. In Oklobdzija, when all the gates of the pMOS and nMOS transistors are at a high voltage level, the stacked transistor pairs of the first and second logic block do not output a high voltage, but become inactive and go into a high impedance state such that no signal is output. In contrast, the switching transistors of claim 29 have a defined electrical potential when at least one supply voltage is switched off.

Because Oklobdzija fails to disclose the explicitly recited limitations of claim 29, and Matsuzaki does not cure this defect, the combination of Oklobdzija and Matsuzaki does not disclose each and every element of claim 29. As a result, the proposed combination of Oklobdzija and Matsuzaki thus cannot establish a prima facie case of obviousness, and the rejection under 35 U.S.C. § 103(a) should be withdrawn. Moreover, since claims 25, 27, 28, and 34-37 ultimately depend on claim 29, the rejections of claims 25, 27, 28, and 34-37 should also be withdrawn. Accordingly, for at least this reasons, Applicants respectfully request the reconsideration and withdrawal of the rejection of claims 25, 27-29, and 34-37.

Moreover, claims 52 and 53 stand rejected for obviousness under 35 U.S.C. § 103(a) as being unpatentable over Oklobdzija in view of Matsuzaki. Having argued that the combination of Oklobdzija and Matsuzaki fails to disclose all of the limitations recited in claim 29, Applicants note that independent claims 52 and 53 include limitations similar in nature to that found in claim 29. In particular, claims 52 and 53 include the limitation of an edge-triggered flip-flop comprising a plurality of switching transistors for coupling a flip-flop input signal into a storage flip-flop subcircuit. Since Oklobdzija in combination with Matsuzaki fails to disclose this limitation for at least the same reasons discussed above with respect to claim 29, the proposed combination cannot establish a prima facie case of obviousness, and the rejections under 35 U.S.C. § 103(a) should be withdrawn.

Finally, claims 39-44 stand rejected for obviousness under 35 U.S.C. § 103(a) as being unpatentable over Oklobdzija in view of Matsuzaki in further view of Sani. These claims depend, either directly or indirectly, on claim 29. In rejecting claims 39-44, the Office Action relies on the

combination of Oklobdzija and Matsuzaki as disclosing all of the limitations recited in claim 29. As shown above, the combination of Oklobdzija and Matsuzaki in fact does not disclose all of the limitations recited in claim 29. Because the combination of Oklobdzija and Matsuzaki does not disclose all of the limitations recited in claim 29, and Sani does not cure this defect, the combination of the combination of Oklobdzija, Matsuzaki, and Sani does not disclose each and every element of dependent claims 39-44. The proposed combination of Oklobdzija, Matsuzaki, and Sani thus cannot establish a prima facie case of obviousness, and the rejections under 35 U.S.C. § 103(a) should be withdrawn.

In view of the above remarks and amendments, Applicants respectfully that each of the presently pending claims in this application is in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejections of the claims and to pass this application to issue.

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